PCI Express Protocol Analysis, Debug and Compliance

PCI EXPRESS™

Agilent Technologies

Agenda

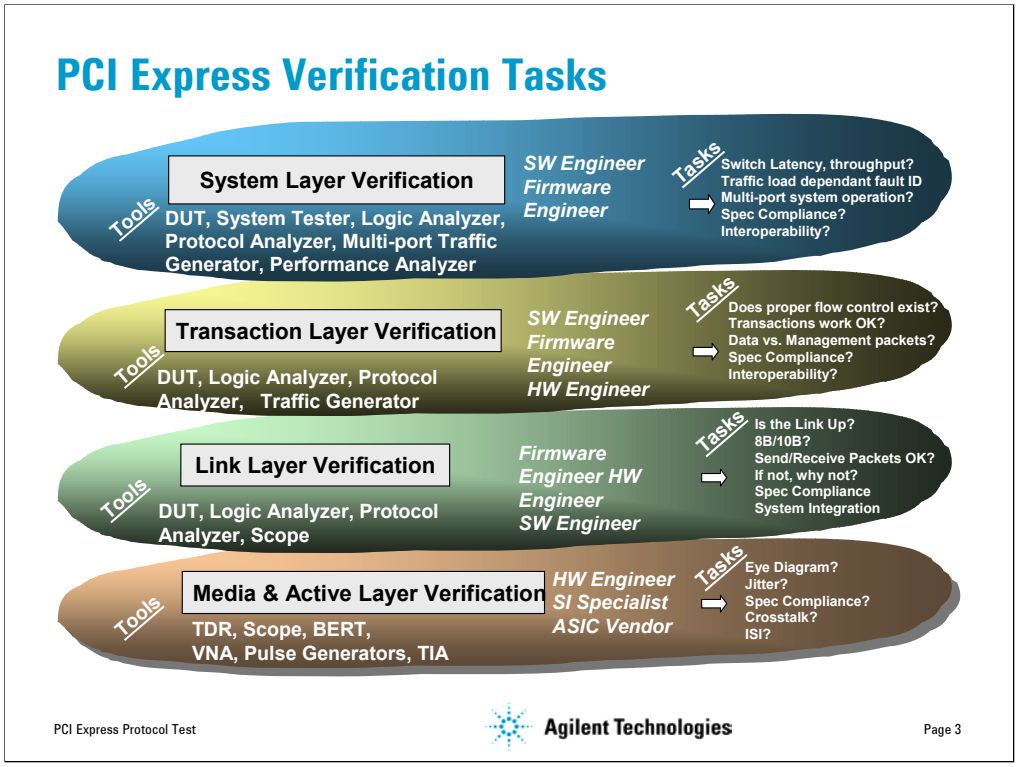
Design Verification Steps

Logic Analysis Tools For PCI Express Development

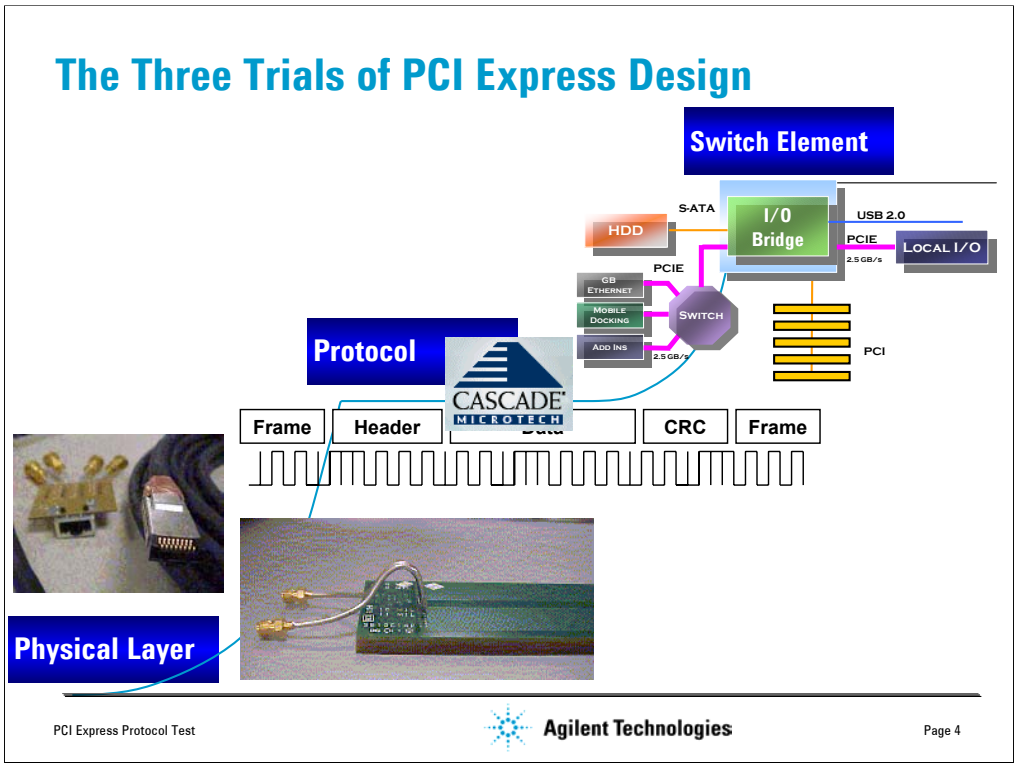
Protocol Tools For PCI Express Development

Summary/Resources

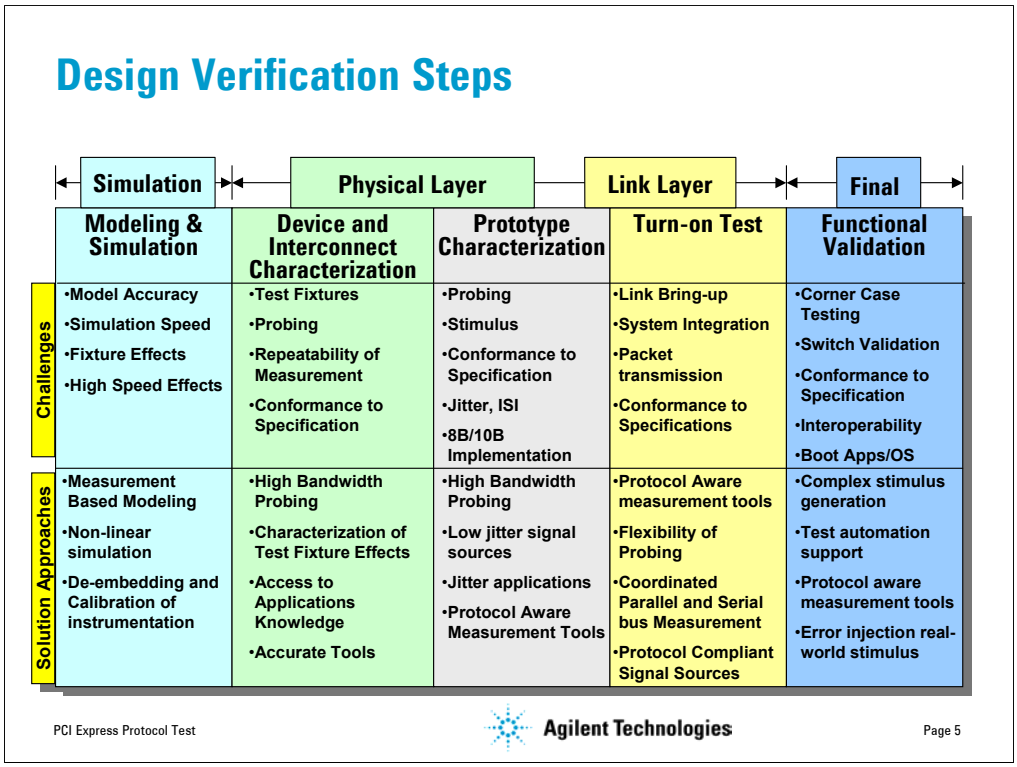
This section will highlight some of the problem areas associated with high speed serial design.



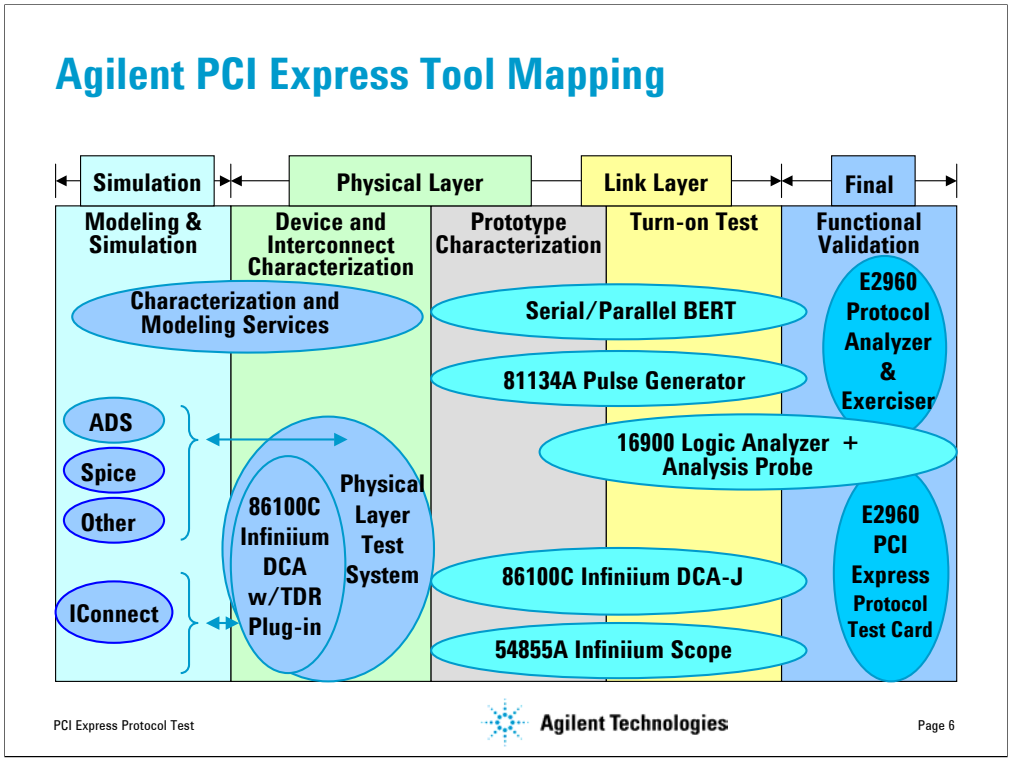
At each layer from the media/physical layer to the system layer, different tasks requiring different tools by engineers with different skill emphasis are required to ensure a properly functioning product.



For Digital Designers there are three new problem areas that you will need to tackle as a result of transitioning to designs using high speed serial interconnects such as PCI Express. With edge rates at 100ps and faster, signal integrity becomes a critical factor in design success. Second, the encoding of data using 8b/10b requires that tools be able to display data in it's native format, preferably showing more than just 0's and 1's. Lastly, the replacement of the multi-drop parallel bus with a sophisticated swtich will require stimulus generation to play a much more active role in system testing and corner case exersizes of traffic on the serial bus.



If we look deeper into what challenges and measurement solutions are required for each of the five phases, we see that Signal Integrity, probing of high speed serial signals, conformance to standards, and interoperability are major challenges. You need the right equipment and measurement expertise to get product to market quickly.



This slide shows how Agilent solutions map to each area of the PCI Express development task flow.

Agenda

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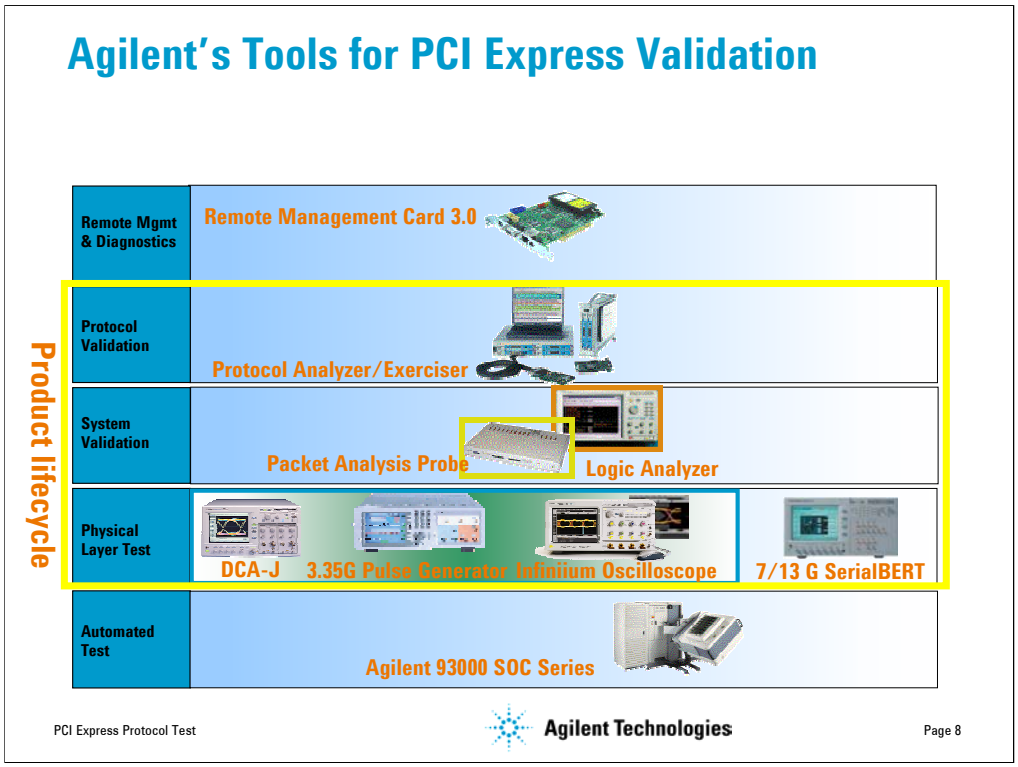
Logic Analysis Tools For PCI Express Development

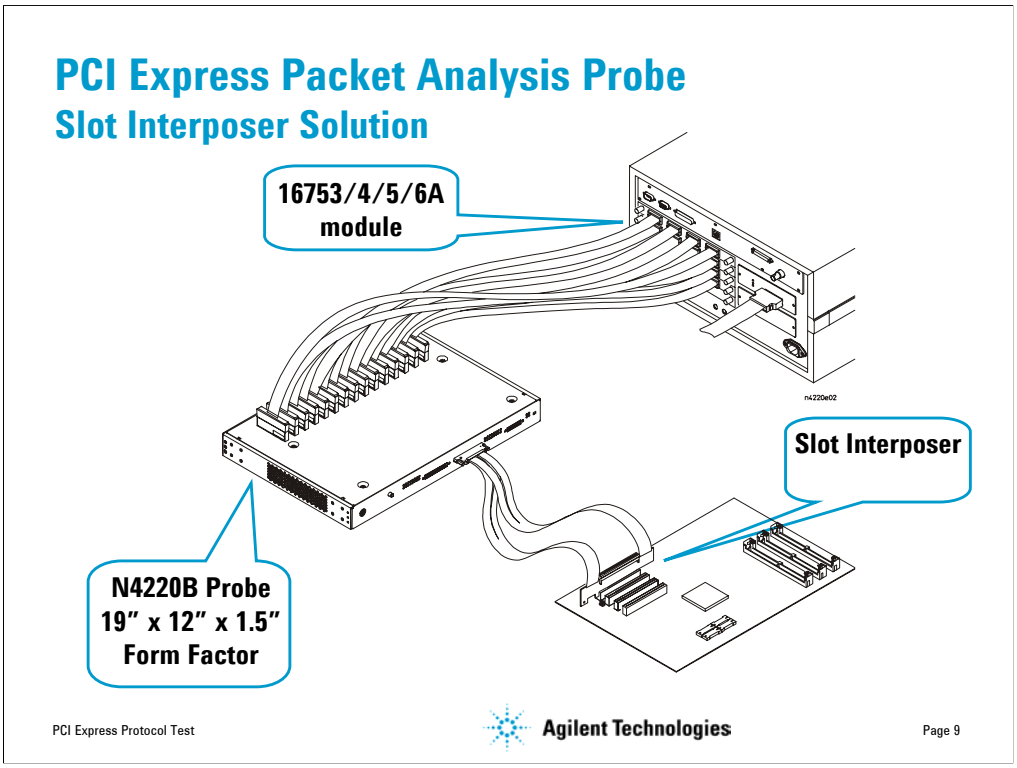
Protocol Tools For PCI Express Development

Summary/Resources

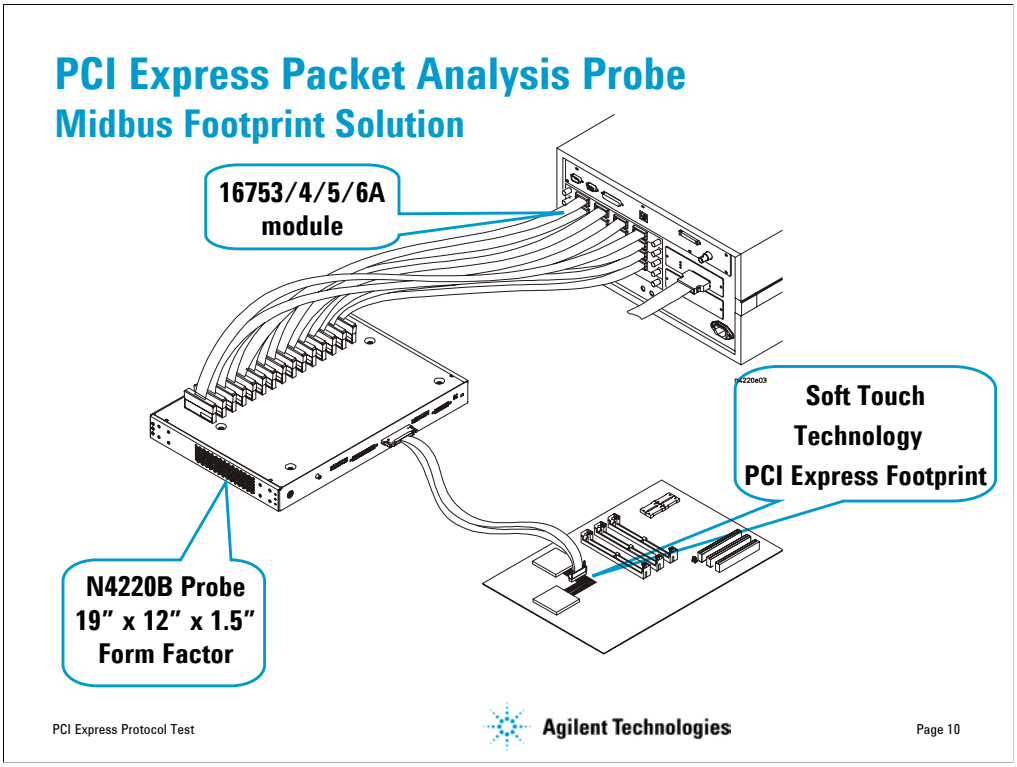
This section will highlight logic analysis solutions for PCI Express.



This section will focus on the system validation aspect of the product lifecycle.



The general look of the logic analysis solution is probing the target system with 1 of 2 types of probes (Mid-bus, Slot Interposer), probe cables extend from the front of the Analysis Probe (a rack mount width, ~1 ft. deep by ~ 1.5 in. high "pizza" box). The 16753 family logic analyzer cables plug directly into the top of the Analysis Probe box along the back without needing an adapter.

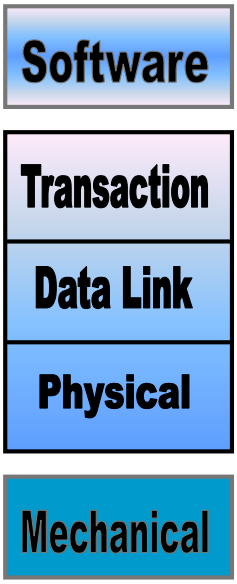


The general look of the solution will be probing the target system with 1 of 2 types of probes (Mid-bus, Slot Interposer), probe cables extend from the front of the Analysis Probe (a rack mount width, ~1 ft. deep by ~ 1.5 in. high "pizza" box). The 16754 family logic analyzer cables plug directly into the top of the Analysis Probe box along the back without needing an adapter.

Mid-bus (a connectorless solution) can be used in in chip-to-chip applications (where no end connection is available).

Digital Validation for PCI Express using Logic Analysis

- **Probing**
  - Non Intrusive observation of data flow
  - Validation of PCI-Express Devices, Add-in Cards, Systems and Chip-to-Chip Architectures
- **Packet Analysis and Display**
  - Dedicated Packet Triggering
  - Software Decode Tool
- **Full System Validation**
  - Cross-Bus Analysis (Time Correlated)
  - Cross-triggering correlation between scope and analyzer



The Agilent logic analysis solution for PCI Express. Our packet analysis probe adds value when validating anywhere from the physical and transaction layers.

N4220B Probe Specs/Requirements

Logic analyzer support

- 16700B or 16702B
  - 16753-series modules
- 16900A or 16902A
  - 16753-series modules or 16950A modules

Extremely fast lock time

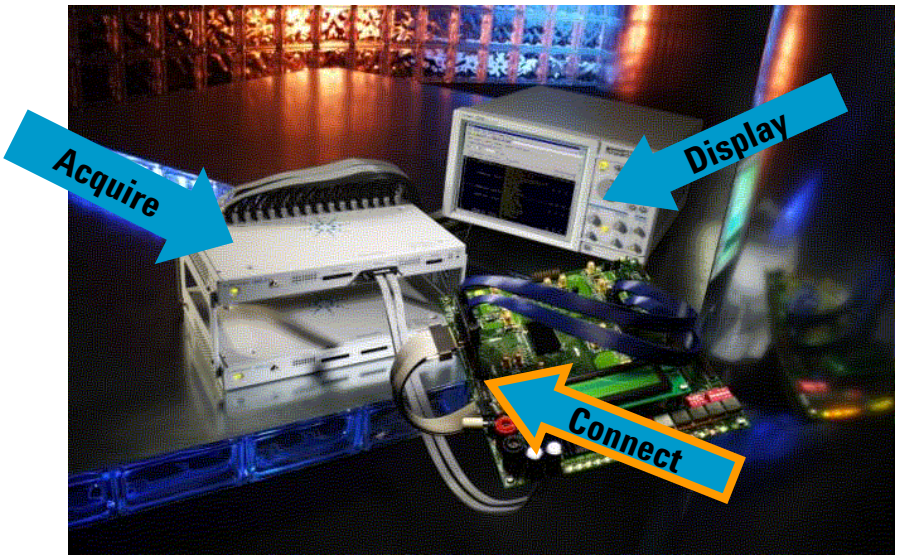
- Requires 12 Fast Training Sequence Ordered Sets for bit/frame sync (48 symbols)

Industry best jitter tolerance

- Minimum eye width of 120ps

Here are the key specs for the N4220B probe.

Logic Analysis PCI Express Validation Steps



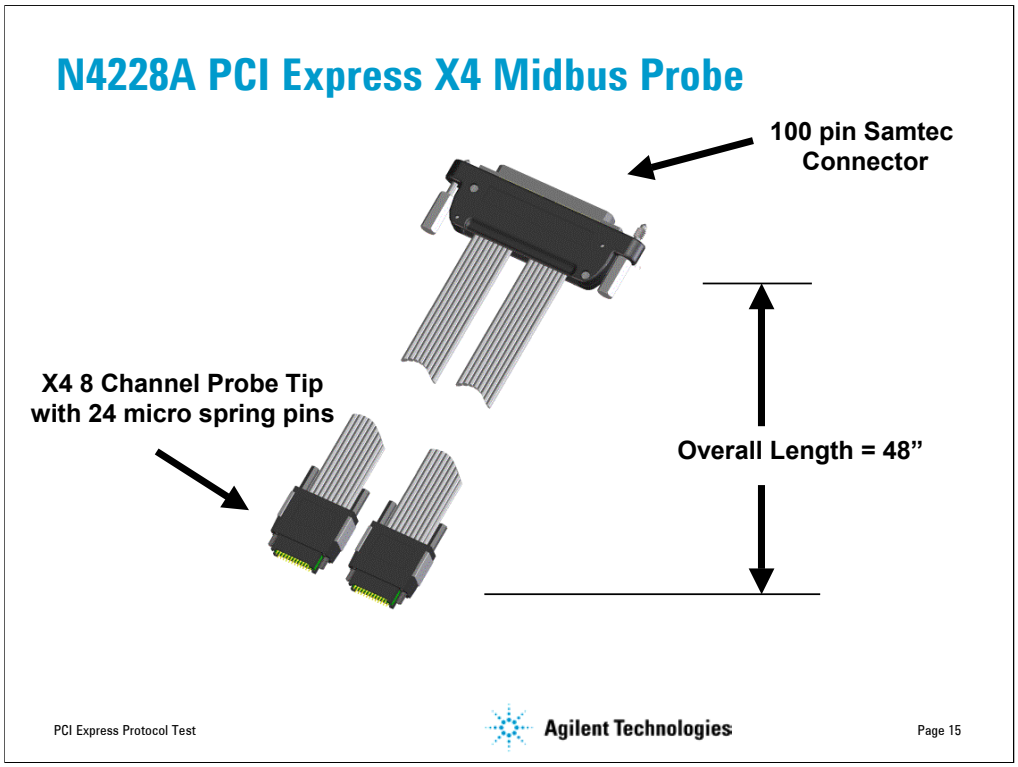
Let's look at the first of three system issues – Connecting to our device.

Connect: Low Intrusion is a must

Types of connection

- **Chip-to-Chip Link – PCI Express footprint**
  - **Soft Touch technology**
- **Card Edge**
  - **Slot connector/interposer**
- **Flying Lead**

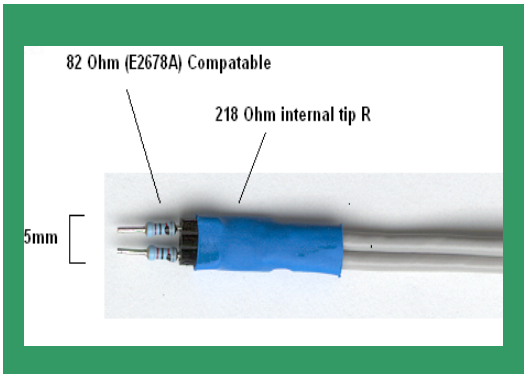
There are several types of connections that can be made to a PCI-E link. For chip-to-chip links, there is a standard PCI-Express footprint that Agilent probes using our soft touch technology. For card edge applications, we offer what is commonly called an interposer, or sometimes called a slot connector. And for applications where there is no place to probe, we offer a flying lead probe that allows access to the 2.5Gb/s data.



The N4228A is a half size midbus cable that is ideal for x1, x2 and x4 lane widths where board space is at a premium. It is the smallest probe available on the market today.

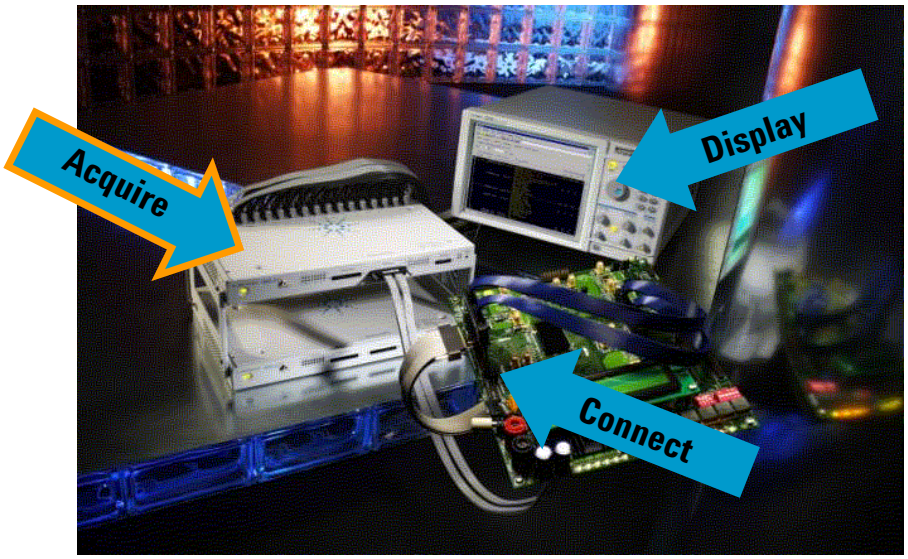
N4221F Flying Lead Set

- **Probing of Individual Lanes regardless of routing**
- **Small KOV**
- **Small Loading**
- **InfiniiMax Compatible**

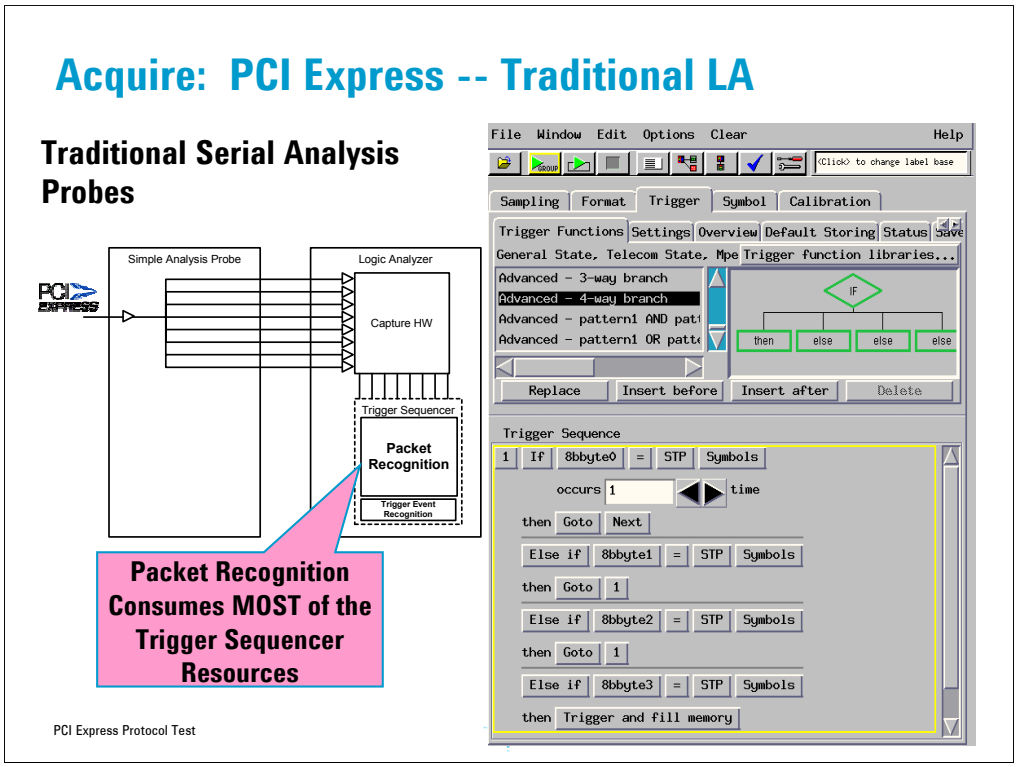


The flying leadset is ideal for customers who may have no board space for a midbus footprint, or who's midbus footprint may have accidentally disappeared between board revs. It provides full speed access to the 2.5Gb/s, and is small enough to probe in extremely tight spaces. It provides support for up to x16 PCI-E, and has the added benefit of being compatible with the Infiniimax scope probes as well (they both use the same 82-ohm resistors).

Logic Analysis PCI Express Validation Steps



Let's look at the second of three system issues – Acquiring the signals.



8bbyteX indicates the lane in which the packet starts.

In a x16 configuration, packets may start on lane 0, 4, 8, 12 (represented by 8bbyte0, 8bbyte1, 8bbyte2. 8bbyte3, respectively)

To dramatically increase triggering capability, we are putting 4 programmable Packet level recognizers into the LAI box for each direction of a link (8 total). These recognizers can be programmed to look for matches to fields within the packet header as well as the first 5 bytes of the data payload. The box will then send simple event recognition notification back to the LA, which can then do full sequencing on those event inputs.

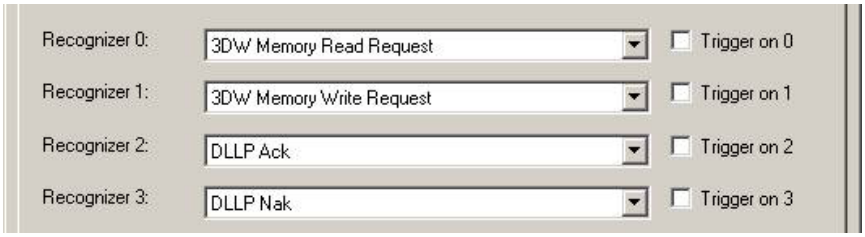
An example: trigger on “packet A” inbound followed by “packet B” outbound followed by “packet C” inbound.

The packet recognition setup is done thru an easy to use hierarchical GUI on the LA to set different fields within a packet to specific values or “Don’t care”.

Acquire: PCI Express Packet Recognition

Enhanced Trigger Capability Through Agilent Packet Recognition

- **8 Header Recognizers will exist in the Analysis Probe (4 Tx/4 Rx) – Implemented in hardware, includes GUI**
  - **24 Bytes in each Header Recognizer (Recognition into Data Portion)**
  - **Recognizers send simple event notification back to Logic Analyzer**
- **Full, Robust Logic Analyzer Sequencing will be available on event notification bits.**



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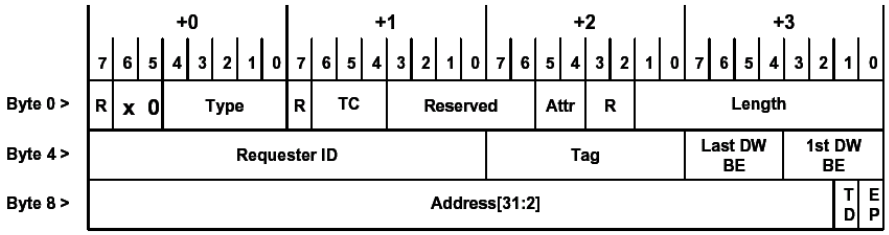
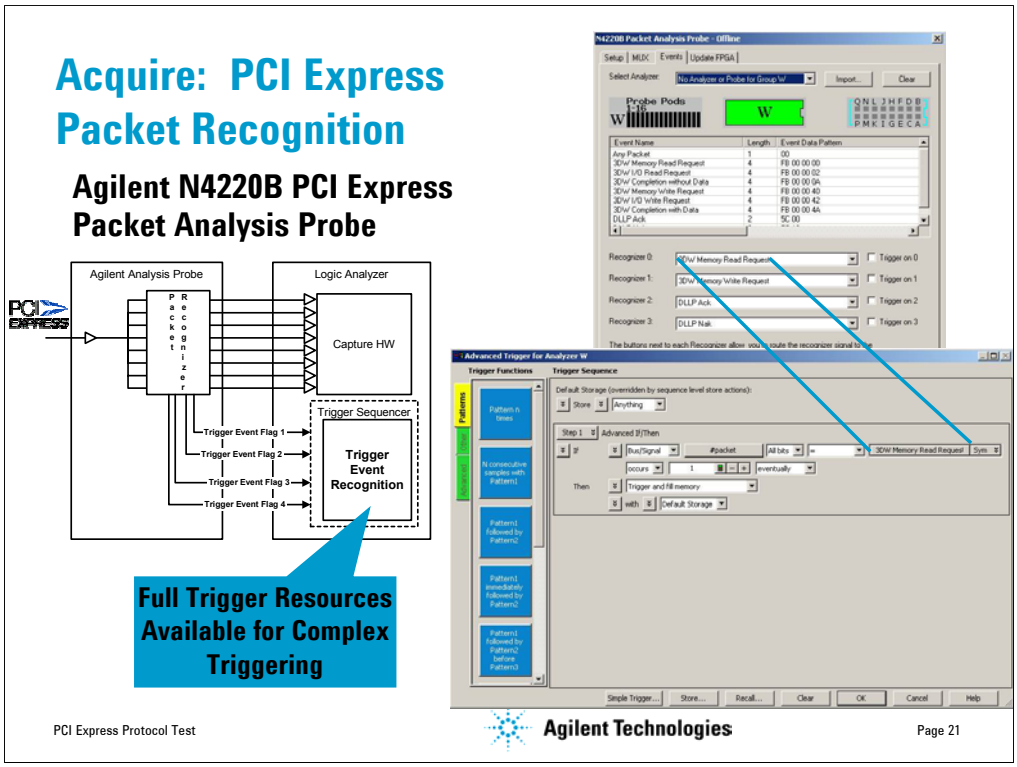
Acquire: Defining a Packet

- ***Describe your trigger at Packet Level***
- ***Analyzer handles bit order, 10B/8B, scrambling, etc.***

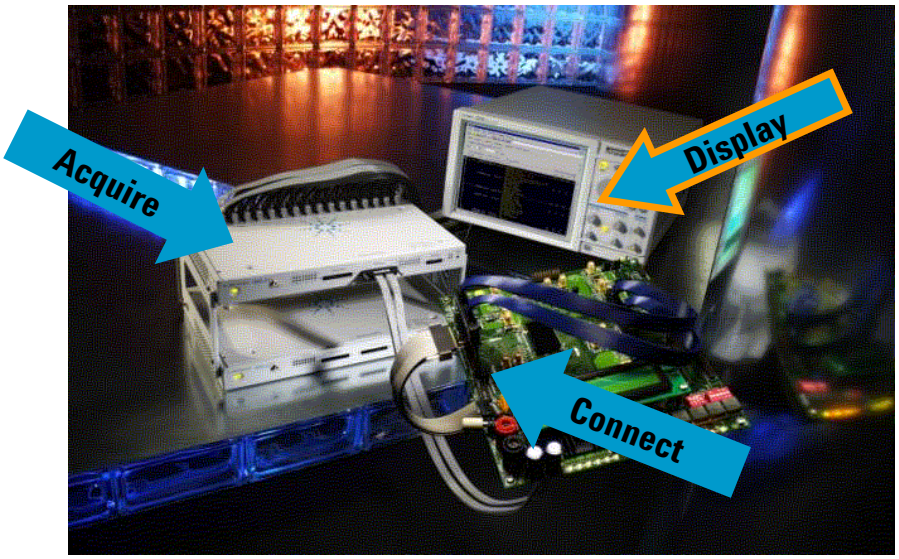


The N4220B allows you to define your packet header with great detail (up to 24bytes) for very precise triggering and searching. The N4220B also handles all of the bit ordering, scrambling, 8b/10b encoding, etc.



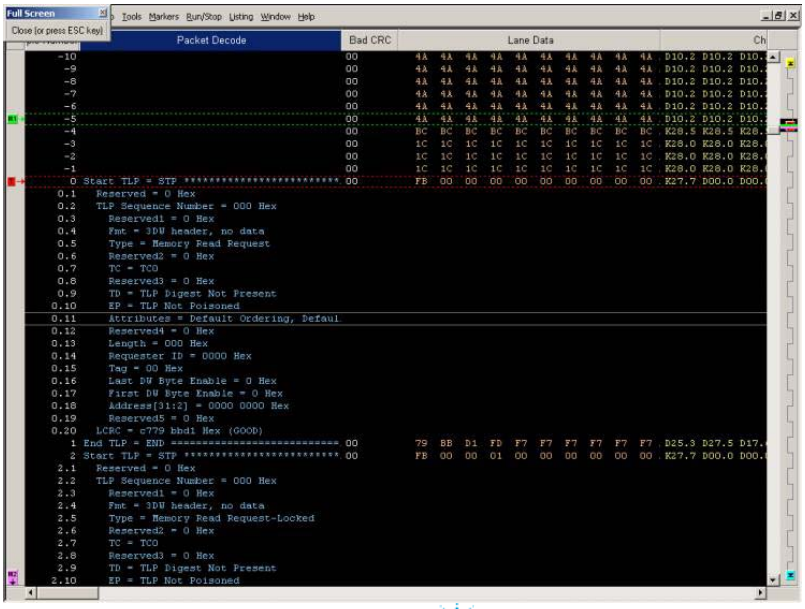
This gives you an idea of how the packet recognizers work. When you compare this to the slide three before this one, you can see how much easier it is to trigger on a complex packet, and how it does not consume the logic analyzer resources (which is especially important for the larger lane widths where a packet can start in multiple lanes and the trigger must look for it in each of those lanes). Each N4220B has four of the packet recognizers per direction built-in to it (for a total of 8).

Logic Analysis PCI Express Validation Steps

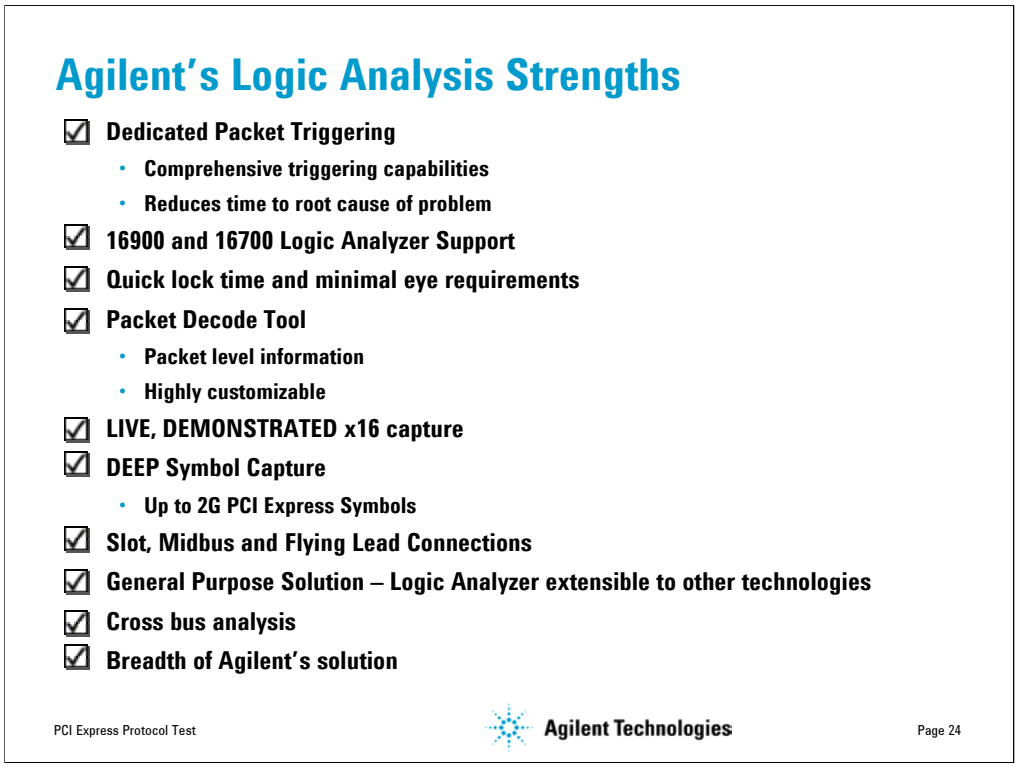


Let's look at the third of three system issues – Displaying the signals.

Display: Packet Decode



This slide gives an overview of the decode that is offered by the logic analyzer. Each packet is displayed in the "packet decode" label with its full content listed. It also offers a "lane data" label that provides the traffic in each lane; a "character names" label that gives the k and d codes; and a "lane decode" label that decodes the k/d codes (i.e. TS1, TS2, SKP, COM, etc.).



In summary, Agilent's Logic Analysis solution for PCI Express offers many important benefits.

Agenda

Design Verification Steps

Logic Analysis Tools For PCI Express Development

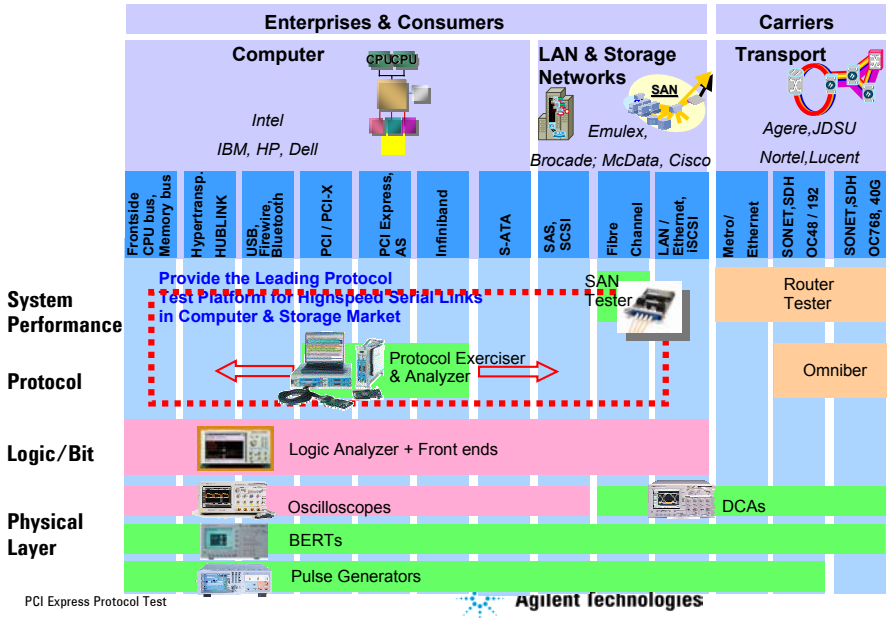
Protocol Tools For PCI Express Development

Summary/Resources

This section will highlight Agilent's protocol tools for PCI Express.

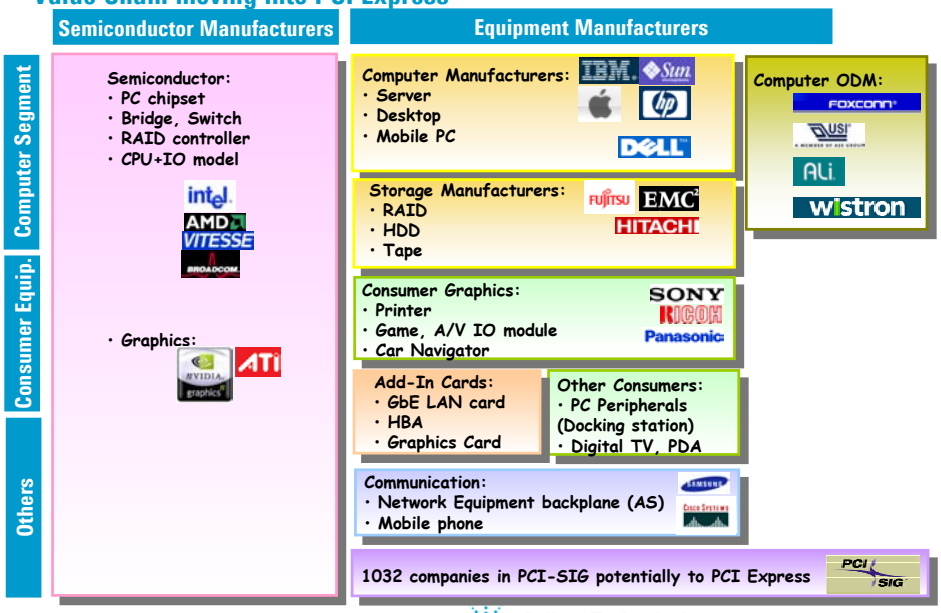
Protocol Test Solutions

PCIE and Fibre Channel Exerciser/Analyzer/Compliance Test



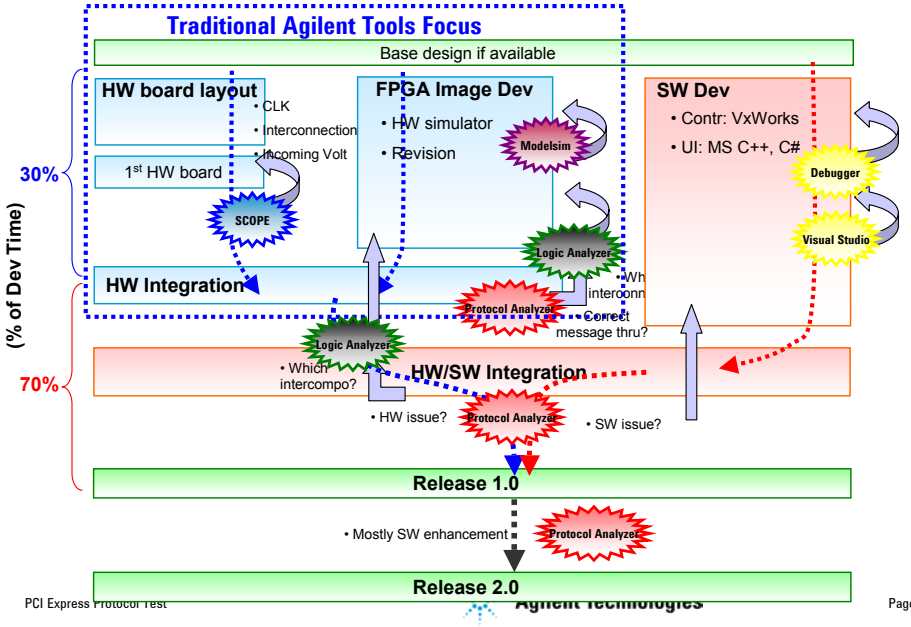
PCI Express Applications

Value Chain moving into PCI Express



Test Tools used by Development Phase

Network Device development example



Protocol Test Solutions: Only Vendor with...

PCI Express Exerciser/Analyzer/Compliance Test

Protocol Test Card:
- Compliance Test
- Jointly Dev. W/ Intel
- GUI/push-button, Pre-programmed tests, Pass/Failed report

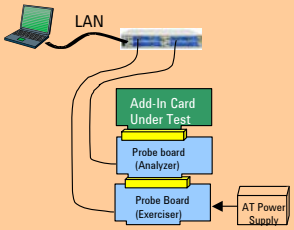
Exerciser:
- Generating and responding on arbitrary bus traffic fully controllable
- CAPI,TCL, GUI
- Testing the error behaviour
- Compliant to defined standards
- Device emulation

Analyzer:
- Patented Dynamic Triggering
- Root cause and performance analysis
- GUI with trigger, search and filter capabilities to intuitively interpret PCI Express traffic

Use Models

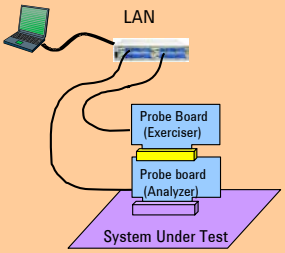
Single probing solutions for both analyzer/exerciser

Add-In Card test w/ Combo solutions



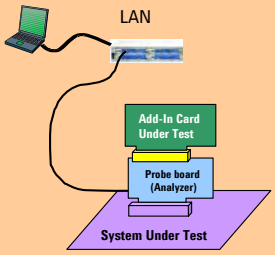
- Protocol Analyzer monitoring bi-directional traffic between Add-in DUT card and known PCIe system
- Protocol Exerciser emulating a known PCIE system device

System Test w/ Combo solutions



- Protocol Analyzer monitoring bi-directional traffic between System DUT card and known PCIE Add-in card
- Protocol Exerciser emulating a known PCIE Add-in card device

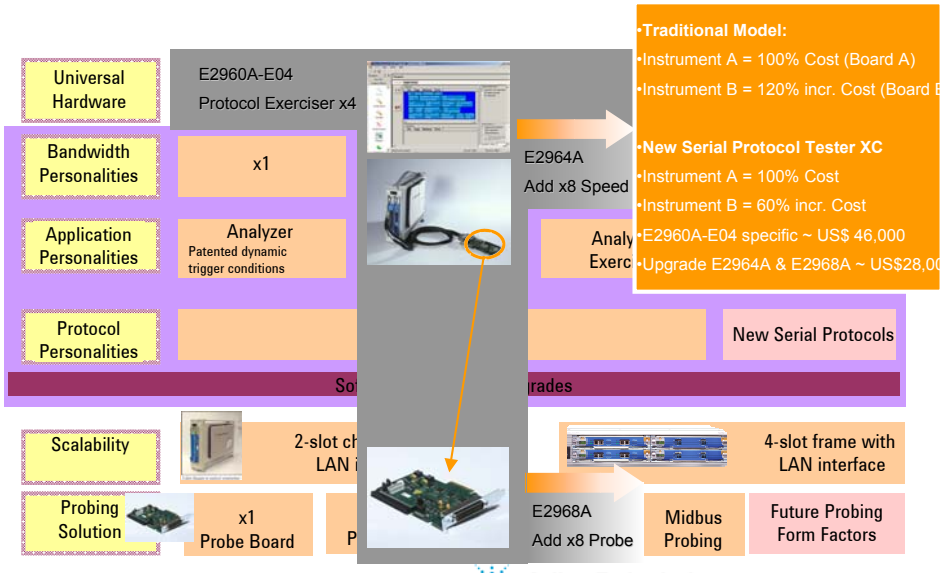
System & Add-In Card Test (PTC)



- Protocol Analyzer monitoring bi-directional traffic between Add-in DUT card and a system DUT
- Protocol Test Card (PTC) validating protocol compliance together

Scenario: Bandwidth Upgrade

Instrument = PCI E Exerciser from x4 to x8 support



Protocol Exerciser and Analyzer Key Capabilities

Overview

Analyzer

- Patented Dynamic Triggering
- Root cause and performance analysis
- GUI with trigger, search and filter capabilities to intuitively interpret PCI Express traffic
- Key tool to Debug and bring up PCI Express designs more easily and faster

Exerciser

- Generating and responding on arbitrary bus traffic fully controllable with the protocol exerciser
- GUI, CAPI and TCL Interface
- Testing the error behaviour of designs by inserting protocol variations with errors
- Supports to be compliant to the industry wide defined standards to validate debug and bring up PCI Express designs easier and faster
- Emulation of devices and automated protocol checking

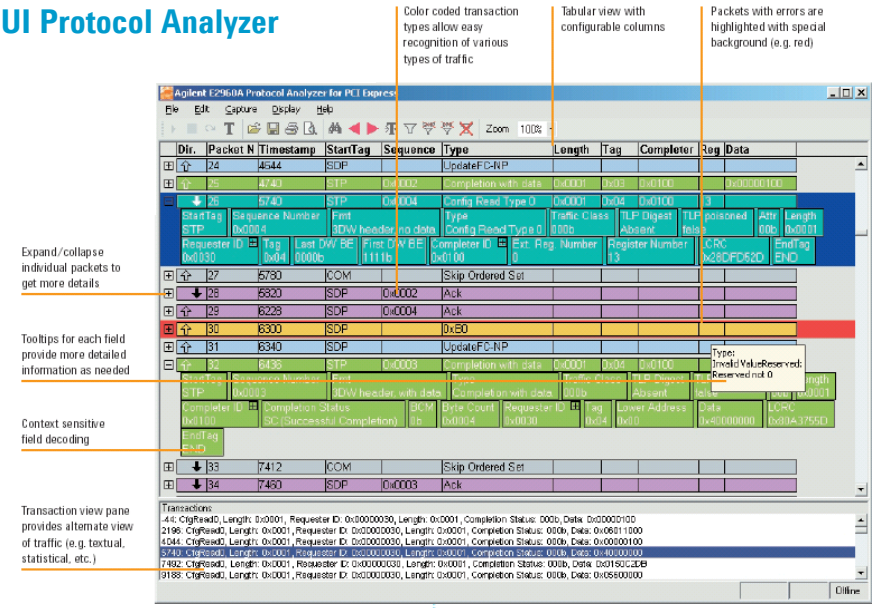
Protocol Analyzer Key Features

Bring up PCI Express designs fast down the design food-chain

- Non-intrusive ("snooping") Protocol Analyzer supporting PCI Express **x1, x2, x4 and x8**
- Supports Specification **1.0 and 1.0A**
- Sophisticated trigger capabilities with patented **Dynamic Triggering** and storage qualification
- **1GB Trace Memory**
- Root cause analysis
- GUI with **Graphical Trigger setup, search and filter** capabilities to intuitively interpret PCI Express transactions
    - Easy navigation within captured trace
    - Hierarchical view
    - Packet view
    - Transaction view
    - Customizable view of captured transaction
- Analysis of transactions between system and add-in card
- **Slot interposer** probe and soft touch **midbus probe**
- Captures training sequences, Data Link Layer Packets and Transaction Layer Packets - Both directions simultaneously, interleaved display, including time-stamps
- **LAN interface** for remote control and to share applications
- **FPGA based** to easy update

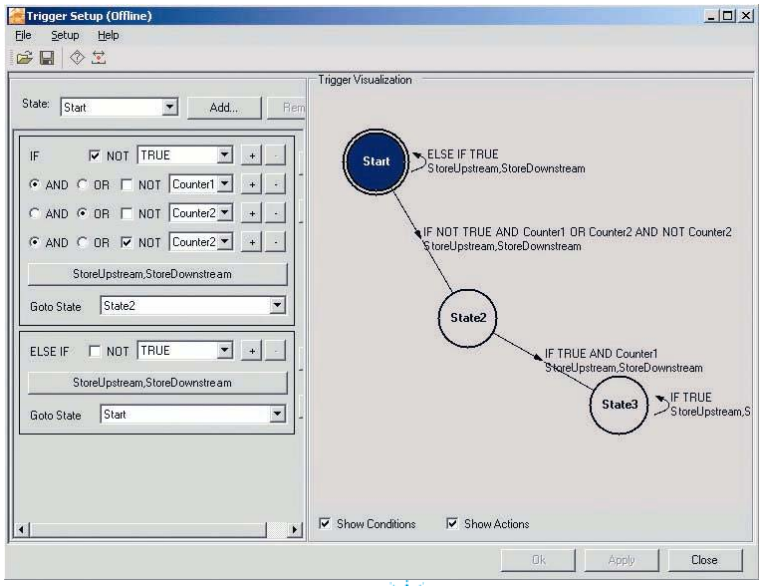
Protocol Analyzer Key Features

GUI Protocol Analyzer



Protocol Analyzer Key Features

Trigger Setup Window - With Visual Sequence Viewer



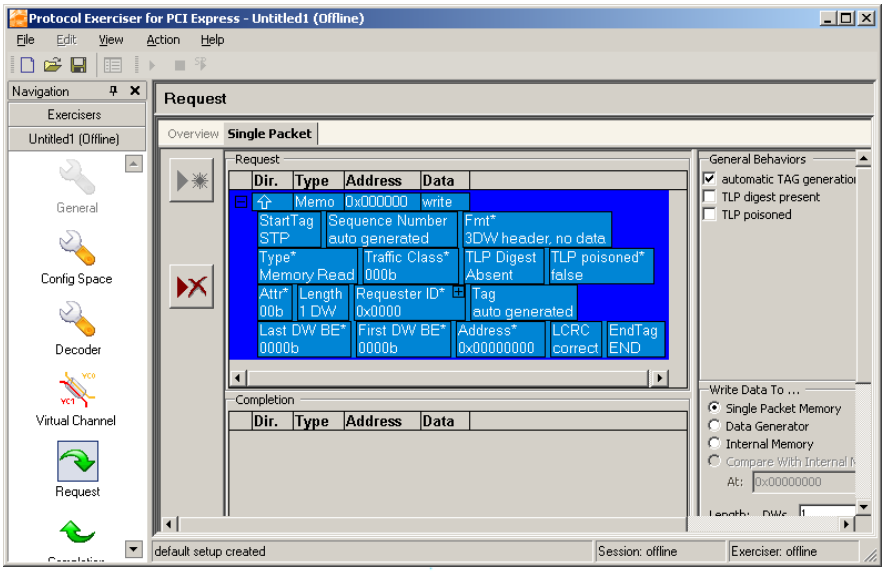
Protocol Exerciser Key Features

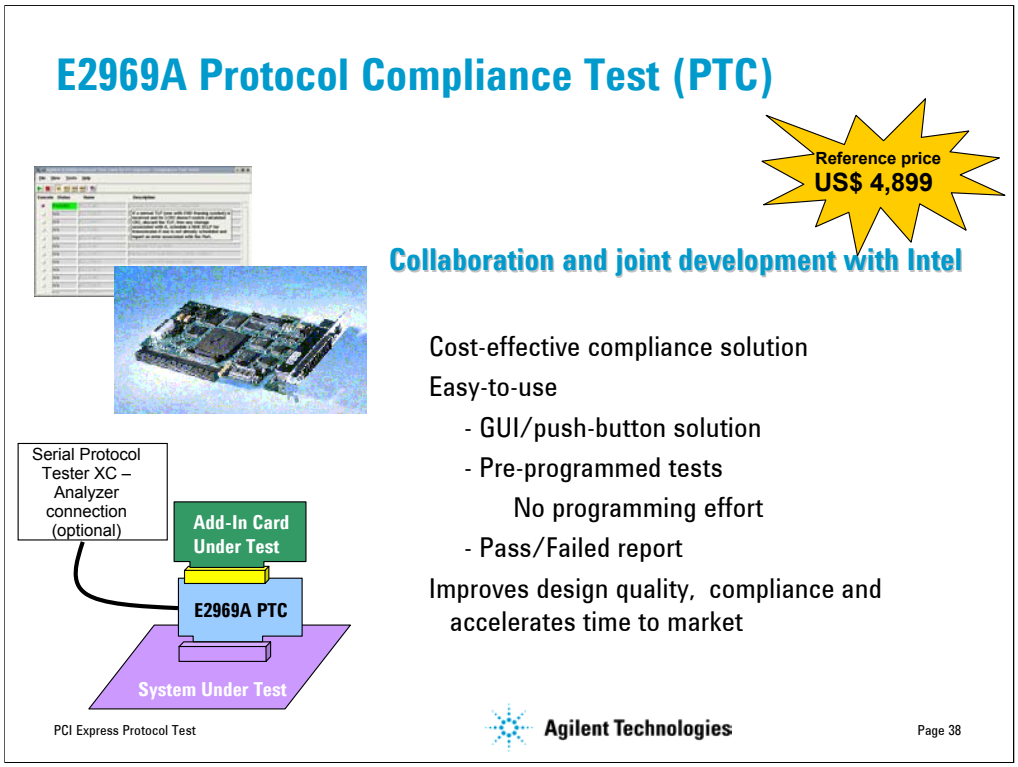
Bring up PCI Express designs fast down the design food-chain

- PCI Express Spec. Rev 1.0 and 1.0a (switchable w/o FPGA Reload)
- Supporting PCI Express x1, x2, x4 and x8
- Supports Specification 1.0 and 1.0A
- 2 M of data memory
- Transmits and receives PCI Express traffic at full bandwidth
- Generate single packets or sequences of packets
- Responds autonomously to incoming requests
- Controlled via GUI, DCOM or TCL interface
- Record and replay Analyzer and Exerciser
- Error Insertion
- LAN interface for remote control and to share applications
- FPGA based to easy update

Protocol Exerciser Key Features

GUI - Inject what you need to DUT





Protocol Test Card for easy and cheap compliance testing to help enable the PCI Express market

The Agilent E2969A protocol test card performs tests to verify and ensure compliance with PCI Express as defined by the PCI-SIG. In addition, the card also guarantees the interoperability of the DUT with other PCI Express devices. It is primarily for use by R&D engineers who wish to validate the functional compliance of their PCI Express-based designs, including chips, add-in cards or systems.

The protocol test card is a collaborative development between Agilent and Intel that coincides with the Intel product development solution for enabling the PCI Express market.

The objective of the card is to give each engineer working on PCI Express designs the possibility to easily and inexpensively test compliance to the standard of the design without any programming effort.

It offers automated pre-programmed compliance tests for the transaction and data link layer and connection to the protocol analyzer

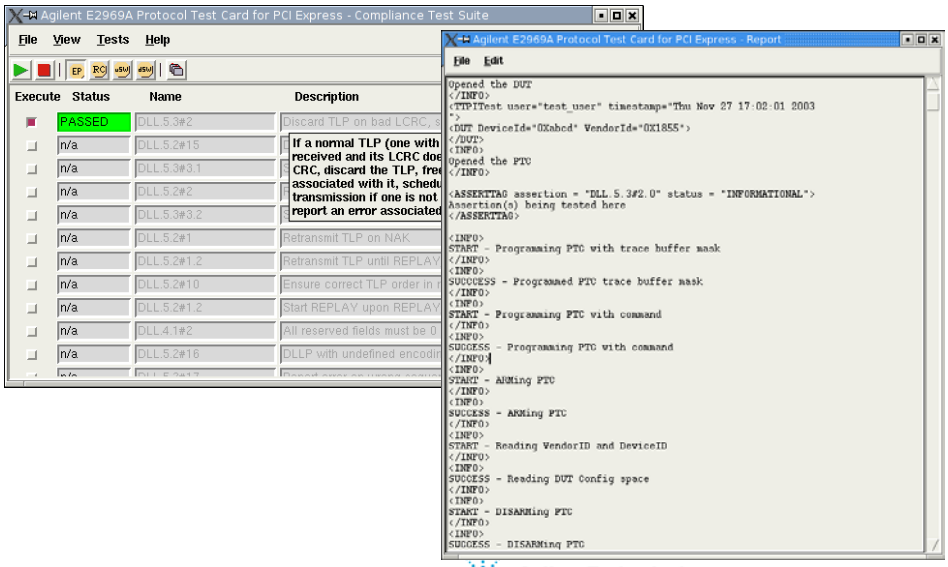
The PTC is field upgradeable FPGA-based card and offers a USB 2.0 interface for programming and topology simulation mode.

It supports add-in cards with up to x16 lane width

The protocol test card provides three test modes. During the add-in card test mode, the card is plugged in between the system and the add-in card. It monitors the behaviour of the add-in card, its device drivers and operating system in response to a range of inserted errors. The platform test mode monitors the behaviour of the platform, its device drivers and OS, also in response to various error conditions. During the topology simulation mode, the protocol test card appears as a complex PCI Express topology. It aids in verifying the PCI Express compliance of the BIOS, so that it is able to detect and initialize a complex PCI Express topology.

E2969A Protocol Compliance Test (PTC)

PTC GUI – main view and Report view



CAPI Leverage Summary

- The objective of the CAPI is to provide the maximum flexibility through our hardware architecture and programming model
- API has been evolved and optimized to meet the new serial protocol aspects
  - Serial protocol parameters are comprehensively addressed
  - Some parameters are not applicable any more (termination, ...)
- Architecture and Resources are similar to PCI
- Programming Model is identical
  - Block / Behavior programming
  - Property concept

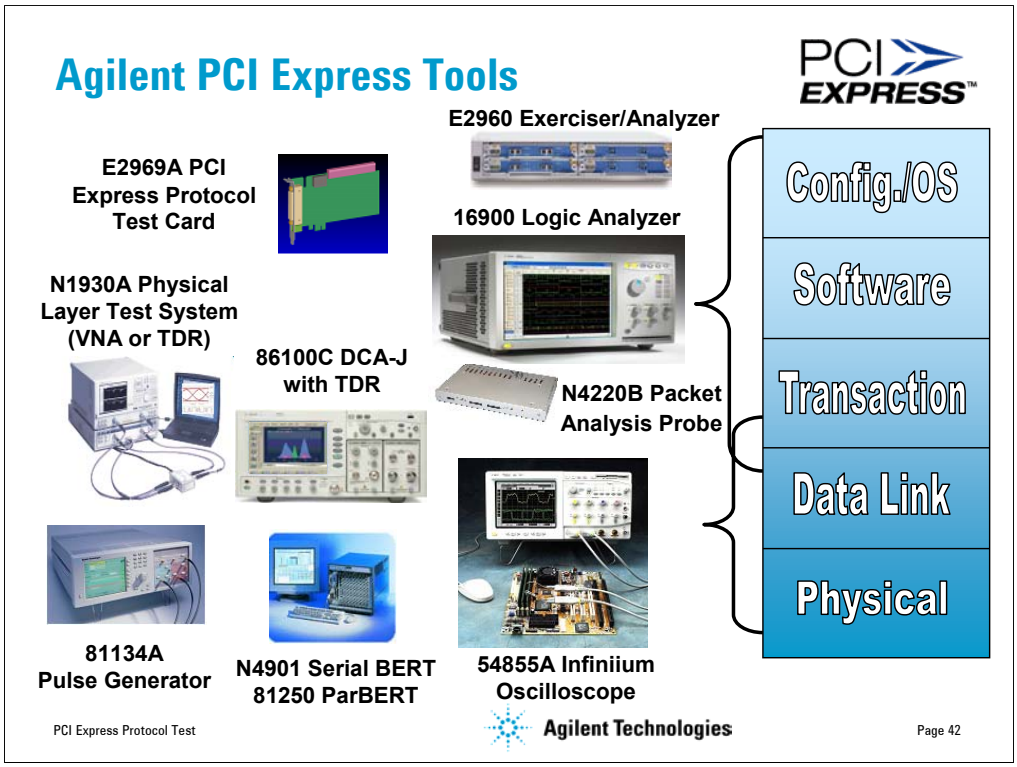
→Programming expertise can be leveraged to 100%

→Similar to moving from PCI to PCI-X

Agenda

- Design Verification Steps
- Logic Analysis Tools For PCI Express Development
- Protocol Tools For PCI Express Development
- **Summary/Resources**

This section will highlight some web resources for PCI Express.



Agilent is ready now with solutions to address problems across the entire spectrum of the PCI express application space. From physical layer testing to application testing.

Resources

PCI Express Products & Application Info
www.agilent.com/find/pci_express

Signal Integrity Application Info
www.agilent.com/find/si

PCI SIG
www.pcisig.com

Agilent's list of application information is continually growing. See the web site on this slide for the lastest information on application notes, design guides, and solution information for PCI Express deployment.